FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	ATTY. DOCKET NO. **ALT-195 CON**	APPLICATION NO.
	APPLICANTS **Edward Flaherty et al.**	CONFIRMATION NO.
	FILING DATE **Herewith**	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
NL	5,432,719	07/11/95	Freeman et al.			
	5,703,759	12/30/97	Trimberger			
	5,781,756	07/14/98	Hung			
	5,787,007	07/28/98	Bauer			
	5,949,987	09/07/99	Curd et al.			
	6,046,603	04/04/00	New			
	6,054,871	04/25/00	New			
	6,085,317	07/04/00	Smith			
	6,215,326	04/10/01	Jefferson et al.			
	6,307,877	10/23/01	Philips et al.			
	6,408,432	06/18/02	Herrmann et al.			
NL	6,628,656	09/30/03	Raza			

FOREIGN DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
NL	Jonathan Rose et al., "Architecture Of Field-Programmable Gate Arrays," Proceedings of the IEEE, vol. 81, No. 7, pp. 1014-1041, July 1993.
	F. Zlotnick et al., "A High Performance Fine-Grained Approach To SRAM Based FPGAs," Wescon '93 Conference Record, September 28-30, 1993, pp. 321-326.
	A. McKenzie et al., "A Versatile Application Bootload for Field Programmable SOC," Technical Developments, Motorola, Inc., Schaumburg, IL, Vol. 39, September 1999, pp. 77-79.
NL	R. May et al., "FPGA Configuration Data Manipulation," Technical Developments, Motorola, Inc., Schaumburg, IL, Vol. 39, September 1999, p. 80.

EXAMINER [signature] DATE CONSIDERED 04/12/06

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

Express Mail
EH623266586US